Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) The ~~A~~ piezoelectric device according to claim 22, ~~comprising:~~

~~a semiconductor integrated circuit having a plurality of bumps formed thereon; and~~

~~a piezoelectric resonator element, the semiconductor integrated circuit and the piezoelectric resonator element being included in a package,~~

~~the semiconductor integrated circuit being mounted in a center of an opening formed in a center of a base, and the semiconductor integrated circuit being connected to an input/output electrode pattern on the base through the plurality of bumps, and~~ wherein the base includes a layered part, which surrounds the semiconductor integrated circuit, for mounting the piezoelectric resonator element, the layered part comprising at least two layers, including a first layer and a second layer, the first layer being below the second layer, wherein an opening of the first layer is formed to be larger than an opening of the second layer.

2. (Currently Amended) The piezoelectric device according to claim ~~1~~ 22, the plurality of bumps formed on the semiconductor integrated circuit being formed at regular intervals on a center portion of an active element surface of the semiconductor integrated circuit.

3. (Currently Amended) The piezoelectric device according to claim ~~1~~ 22, the plurality of bumps formed on the semiconductor integrated circuit being concentrically formed about a center of an active element surface of the semiconductor integrated circuit.

4. (Currently Amended) The piezoelectric device according to claim ~~1~~ 22, further comprising a dummy bump formed on an active element surface of the semiconductor integrated circuit.

5. (Previously Amended) The piezoelectric device according to claim 4, the dummy bump formed on the semiconductor integrated circuit being connected to the electrode pattern on the base.

6. (Canceled)

7. (Canceled)

8. (Canceled)

9. (Canceled)

10. (Canceled)

11. (Currently Amended) The piezoelectric device according to claim ~~10~~ 14, the protrusion being formed in each of side walls of the base facing two sides along the longitudinal direction of the semiconductor integrated circuit.

12. (Currently Amended) The piezoelectric device according to claim ~~10~~ 14, the protrusion formed in the side wall of the base having a substantially same height as, or is higher than, the semiconductor integrated circuit.

13. (Currently Amended) The piezoelectric device according to claim ~~10~~ 14, wherein a gap between the protrusion formed in the side wall of the base and the semiconductor integrated circuit being set to a range between 0.05 and 0.15 mm.

14. (Currently Amended) The ~~A~~ piezoelectric device according to claim 22, ~~comprising:~~

~~a semiconductor integrated circuit; and~~

~~a piezoelectric resonator element, the semiconductor integrated circuit and the piezoelectric resonator element being included in a package,~~

~~a plurality of bumps being formed at two opposing sides of an active element surface of the semiconductor integrated circuit, the semiconductor integrated circuit being mounted in an opening formed in a center of a base, and the semiconductor integrated circuit being connected to an input/output electrode pattern of the base through the plurality of bumps, and~~ a protrusion being formed in at least one side wall of the base facing the side of the semiconductor integrated circuit and protruding into the opening to form the protrusion.

15. (Canceled)

16. (Canceled)

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Canceled)

21. (Canceled)

22. (Previously Amended) A piezoelectric device, comprising:

a semiconductor integrated circuit; and

a piezoelectric resonator element, the semiconductor integrated circuit and the piezoelectric resonator element being included in a package,

a plurality of bumps being formed at two opposing sides of an active element surface of the semiconductor integrated circuit, the semiconductor integrated circuit being mounted in a center of an opening formed in a center of a base, and the semiconductor integrated circuit being connected to an input/output electrode pattern through the plurality of bumps by ultrasonic bonding, each of the plurality of bumps formed on the semiconductor integrated circuit being shaped to have two levels, a first level having a diameter 0.8 to 0.9 times and a second level having a diameter 0.4 to 0.45 times the length of an opening in a pad provided on the active element surface of the semiconductor integrated circuit.

23. (Previously Amended) The piezoelectric device according to claim 22, a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit being perpendicular to two opposing sides of the active element surface of the semiconductor integrated circuit at which the plurality of bumps are formed.

24. (Previously Amended) The piezoelectric device according to claim 22, a printing direction of the electrode pattern on the base being the same as a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit.

25. (Canceled)

26. (Previously Amended) The piezoelectric device according to claim 22, wherein the first level is 80 to 90 μm in diameter and 30 to 35 μm in height, and the second level is 40 to 45 μm in diameter and 30 to 35 μm in height.

27. (Previously Amended) The piezoelectric device according to claim 22, the base comprising a ceramic composite substrate.

28. (Previously Amended) The piezoelectric device according to claim 22, the plurality of bumps formed on the semiconductor integrated circuit being Au bumps.

29. (Previously Amended) The piezoelectric device according to claim 22, a longitudinal direction of the electrode pattern on the base being the same as a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit.

30. (Previously Amended) The piezoelectric device according to claim 22, a vibration direction of ultrasonic waves for ultrasonic bonding and for forming bumps on the semiconductor integrated circuit being different from a vibration direction of ultrasonic waves for performing ultrasonic bonding of the semiconductor integrated circuit to the package.

31. (Canceled)

32. (Canceled)

33. (Canceled)

34. The piezoelectric device according to claim 14, wherein a gap is defined between the protrusion and the semiconductor integrated circuit in that the protrusion does not contact the semiconductor integrated circuit.

35. (Canceled)

36. The piezoelectric device according to claim 34, wherein an underfill material permeates the gap and fills a portion of the integrated circuit having the plurality of bumps.

37. The piezoelectric device according to claim 1, wherein an underfill material permeates to the first layer and fills a portion of the integrated circuit having the plurality of bumps.